Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **CLR 1**
2. **D1**
3. **CLK 1**
4. **PR1**
5. **Q1**
6. **N. Q1**
7. **GND**
8. **N. Q2**
9. **Q2**
10. **PR2**
11. **CLK 2**
12. **D2**
13. **CLR2**
14. **VCC**

**.045”**

**2 1 14 13 12**

**3**

**4**

**11**

**10**

**5 6 7 8 9**

**L0**

**74**

**MASK**

**REF**

**.045”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: L074**

**APPROVED BY: DK DIE SIZE .045” X .045” DATE: 6/18/21**

**MFG: FSC / NSC THICKNESS .014” P/N: 54LSR74**

**DG 10.1.2**

#### Rev B, 7/1